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REVIEW THE TECHNIQUE NEW DOUBLE-TAIL COMPARATOR FOR OFFSET VOLTAGE OPTIMIZATION

Author's Name: [1]Kavindra pal, [2]Mr. Anuj Garg

Affiliation: *[1]Student,Lakshmi Narain College of Technology, Bhopal, Madhya Pradesh, INDIA*

[2]Professor, Lakshmi Narain College of Technology, Bhopal, Madhya Pradesh, INDIA

E-Mail: 0103ec19mt03@lnct.ac.in

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Abstract

In the course of this research and on consideration of the presented results, some prospects for future work and some problems that may be the subject of further study are marked. A few of the directions for are discussed below: To proposed approach for Offset voltage optimization. It will reduce by applying the offset minimizing technique e.g. auto zeroing technique. Our propose technique for power reduction achieve by applying a power reduction technique e.g. adaptive power control. To performing the evaluation between the parameters like kick-back noise reduction and accuracy (dynamic and static offset, noise, and resolution) can be one of the add-ons. To design of ADC can be carried out using presented high speed, low power, and a low voltage dynamic comparator.

Keywords*: Accuracy, Adaptive Power Control,Dynamic Comparator.*

INTRODUCTION

Comparator is one of the main components in most analog to digital converters (ADCs). Many high-speed ADCs, like flash ADCs, demand low-power comparators with a small chip area. In the ultra-deep (UDSM) CMOS technologies, high-speed benchmarks are subject to very low delivery voltages, especially given that system threshold voltage has not been scaled at the same pace as modern CMOS process supply voltages[2].

Therefore, when supply voltage is lower, the architecture of high-speed comparers is more demanding. In other words, in this technology, to achieve high speed, larger transistors are required to compensate the reduction of the supply voltage, which also means the more die area and power is needed. Furthermore, low voltage operation leads to a restricted input range in common mode, which is critical for ADC high-speed architecture, including Flash ADCs. The comparator is a circuit that contrasts an analog signal with an analog voltage or reference voltage and generates a comparative binary signal. Vp is the input voltage (pulse voltage) applied to the positive input terminal of comparator and Vn is the reference voltage (constant DC voltage) applied to the negative terminal of comparator.High speed dynamic regenerative comparators are used in low power and area efficient analog to digital converters to improve speed and power efficiency. Speed and power consumption are the two factors that define the comparators accuracy. A comparator is a devisce that compares two voltages or currents and outputs a digital signal indicating which is larger. In this research work, a new double tail comparator is proposed by modifying the low voltage low power double tail comparator circuit for power efficient and high speed operation. In the proposed dynamic double tail comparator System both the power dissipation and delay time would be significantly reduced. The simulations are carried out in MENTOR GRAPHICS, Schematic editor, Generic GDK, 130nm technology.

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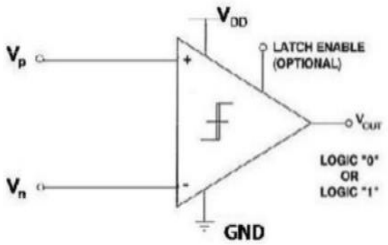

Figure 1: Schematic of Comparator

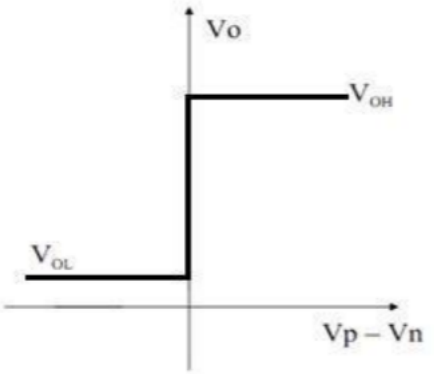

Figure 2: Ideal voltage transfer characteristic of comparator

A clocked comparator is used in two steps. The two entry signals are interfaced in the first level. The second stage is made up of two inverters that connect each input to the other output. In a CMOS-based lock, the renewable phase and subsequent phases use low static
power as either PMOS or NMOS transistors transform the power path[3]. In many applications, power dissipation and transistor count are more essential. If comparator speed is a priority, the regenerative stage could begin operation at the midpoint between power supply and ground. Traditional comparators, for example, can increase transistor count by reducing speed by reducing static power consumption.

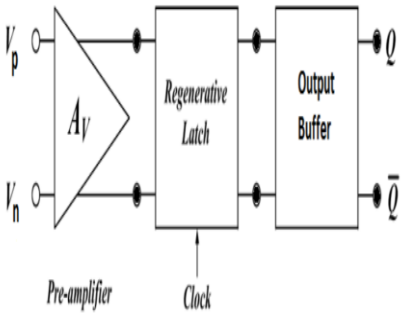

Figure3: Block diagram of Comparator

RELATED WORK

There are several design considerations for comparator design which present the significant static and dynamic qualities of the comparator. The basic types of comparator architecture will

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be subsequently discussed. The various types of comparators are divided into three main groups, namely Open-loop, Pre-amplifier-dependent Latched Comparator and Dynamic Latched Comparator based on a study of the literature. In particular, the various types of dynamic latch comparators and their advantages and drawbacks from literature are presented

Characteristics of Comparator

The fundamental characteristics of the comparator are the two-type types, specifically Static and Dynamic.

Static Characteristics

Static characteristics are used to measure output parameters of constant quantities or variations only very slowly. The following are:

A. Gain
B. Offset Voltage
C. Noise
D. Input resolution
E. Input common mode range (ICMR)

Gain: It is referred to as a comparator's ability to boost the input signal to the output. That is the distinction. The differential output to differential input value ratio is commonly defined. Voltage gain equals total gain in the circuit. Higher benefit means more capacity to solve small signals in many applications. Figure 1 depicts the transition curve of a final gain.

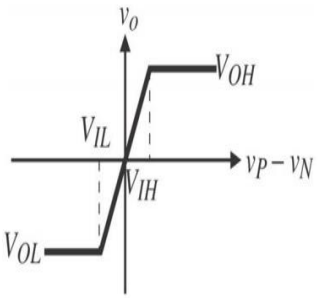

Fig. 4 Transfer curve of a comparator with finite Gain

The gain of a comparator given as

$$Gain\,(A_V) = \lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V}$$

Shows the widespread profit formula (Av). In this case, TV is the input voltage set, VIH is VOH's smallest input value, and VIL is the larger input for which the output voltage is VOL. Gain is generally a very critical description of the function of the comparator. It specifies the minimum input adjustment (resolution) required to swing the output between the two binary states. Input requirements for the digital circuitry regulated by the comparator output typically determine both output state. The voltages VOH and VOL must be adequate to meet the VIH and VIL requirement of the following digital level.

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Offset Voltage: Offset occurs in comparators as a result of transistor mismatches. (There is a discrepancy between the transconductance parameter and the threshold voltages.) It is possible to define the voltage generated by misplacements between input transistors. Threshold voltages for various geometric geometry transistors and transductions vary depending on geometry. It is classified as follows:

a. Systematic Offset - Offset voltage is present if the nominal value has been assumed by all system and model parameters. The designer is almost always responsible for very limited systemic offset voltage.
b. Random Offset - The error voltage is generated as a random offset voltage due to random variants in process parameters and system dimensions. In fact, the random offset is a random design variable,
but is deterministic when produced in any particular unit. It depends heavily on the architecture.
c. Output Offset Voltage - Once the 2 input terminals have grounded it is known as dc voltage on the output terminal of the comparator.
d. Input Offset Current - The voltage of a comparator is determined as the difference between two opposite currents in the input port in order to equal it. e. Voltage Offset Input - To achieve the desired result in output voltage balance between the two inputs, the required input dc voltage differential is used. The input offset voltage (VIO) is the differential input voltage that is applied to the input in order to toggle the output level. The comparator resolution is limited by the voltage of the input offset. Thus, on very little (in the same order as the input offset voltage (VOI)), the comparator changes to an unexpected value or does not turn over at all (Allen et al. 2002). In other words, a voltage source connected in series to an ideal comparator input can represent the input offset voltage. As a result, the output does not change when VIN+ = VIN, as it would with an ideal comparator, but the threshold level is modified when the input offset value VIO is changed. The input offset tension rises as a result of transistor imbalance.

1. In conventional comparators, the mismatch between the cross coupled circuits determine the trade-offs among the speed, offset and the power consumption.
2. Existing state of art comparator architectures are either fully differential design or double tail Design.
3. Design of Tail Transistor: It confines the total current flow through the output branches and demonstrates greater dependency on offset voltage and speed with different values of VCM.
4. The separated output latch stage and input gain stage for low offset voltage and low noise. The comparator operates over a wide range of input common mode voltage at a low supply voltage for low and more stable offset voltage.
5. The previous code dependent errors or decision determines the accuracy and precision of the comparator so, reset strategy is also an important consideration for design of dynamic comparator.
6. For low offset, there should be less stacking of transistors between input transistors and tail transistor.
7. For further reduction in power consumption, comparator architecture should be design with reduce transistor count and minimum hardware.
8. Characterization in terms of offset, propagation delay, ICMR, gain, phase margin, CMRR, PSRR power dissipation, mismatch analysis, process variations were carried out for promising

FDDTDC architectures.
9. Proposed FDDTDC architectures are less sensitive to parameter variations and more stable than existing architecture.

Dynamic Characteristics

The strong positive feedback based dynamic latch clocked comparator is a strong candidate in many high-speed analog-to-digital converters (ADCs) due to its fast decision-making ability. Analysis has been presented in literature, which examine various performance parameters such as kick-back noise. In this section, the functionality of commonly used topologies, i.e. conventional single tail dynamic latch comparator (STDLC), and conventional double tail dynamic latch comparator (DTDLC), modified double tail comparator (MDTDLC), two-stage dynamic comparator without an inverted clock (DTDLC-CLK), and pre-amplifier with latch comparator (Pre+Latch) are presented. The comprehensive analysis of delay is investigated for these generally used topologies. The concept and methods/approach for delay and power reduction is presented. Finally based on these analysis, investigation, and subsequently, its implementation results comparison, a new comparator architecture (i.e. proposed shared charge double tail comparator (PSCDTC)) is proposed. The complete theory and analysis The proposed comparator (Delay, Power, Offset Voltage and ICMR) The value of certain parameters, which varies with time, is defined. A comparator's dynamic properties are: A. Delay in spreading. B. Speed C. Temporary rate D. Electricity use Delay of propagation: this is the delay from input to output. The transition from input through mid-point to mid-point of output as shown in Fig. 5 is measured in comparators (Allen et al, 2002). The delay time of the dynamic comparator (the clocked regenerative comparator) is the minimum time period from the start of the confrontation process (reset when the corresponding clock edge normally exceeds 50% of Vdd). The minimum time period from the beginning of the comparison process (reset when the clock edge usually reaches 50 percent of the Vdd) is also specified, until one output node reaches the half voltage of Vdd/2 (Goll, et al., 2015).

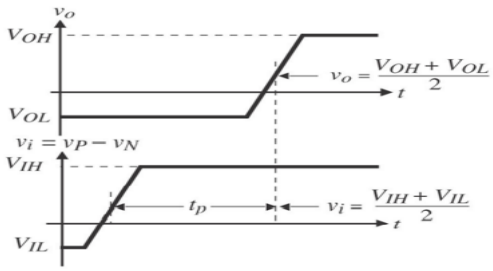

Fig. 5: Input-Output characteristics showing propagation delay of the comparator

PROPOSED METHODOLOGY

The propose comparator is inherited primarily from double tail current based dynamic latch, so it retains all the advantages of the double tail current based comparator. The proposed double tail current dynamic latch comparator uses the concept of shared charge logic as a reset technique for the delay and power reduction with use of a pMOS pass transistor. It possesses better performance than its counterpart architecture. As there are two separate and independent tail currents, optimization can be achieved independently for the performance in terms of delay and power consumption. Moreover, there is no requirement of additional

reset/set transistor(s) as it is required in the other referred comparator architecture to reset/set output terminals during reset/set phase, which ultimately reduces the power consumption and die area. The equation for the delay is derived for the proposed architecture and it is shown that the effective transconductance of the latch (Gm) is increased, which in turn reduces overall delay. Finally, the APC technique for the further reduction in the power is also explored for the future development of the proposed architecture.

The APC circuit can be implemented with only one NAND gate and one inverter. The APC block performs the following functions: Following the evaluation, the output triggers the adaptive power control block. During the reset operation, the clock is set to zero, and the output terminals are powered to Vdd by the reset transistors, while the NAND port output is set to HIGH. When the clock strikes twelve o'clock, the assessment stage begins. As the clock shifts from low to high, the output of the NAND gate decreases. When the evaluation is over, one output terminal is at Vdd and the other is at Ground, and the output of the NAND gate changes to a HIGH state. While the pre-DC amplifier's power control switches are NMOS, the NAND output is reversed such that the ultimate APC signal becomes a transistor input that stops the rail-to-tail connection before a decision is taken.

Advantages of propose approach

These structures have zero static power consumption, a high input impedance, maximum swing efficiency, mismatch robustness, and noise immunity. Because of the parasite's ability to input data. Transistors have no direct effect on the rate at which output nodes are switched, and large transistors can be built to reduce the offset in the input level (different amplifier). On the other hand, it increases electricity and dietary space.

Disadvantages of STDLC Architecture

The disadvantages of the architecture are as follows:

Since there are many stacked transistors, the voltage needed for a proper delay is adequate. This is due to the fact that only two transistors (M3 and M4) are initially turned on before one of the transistors (M5 or M6) is turned on (the voltage level of one output node has dropped below a level, small enough, to turn ON transistors M5 or M6 to start complete regeneration). As a result, a high voltage supply is needed for proper operation. The voltage reduction with a low voltage only provides a slight gate-source voltage to transistors M3 and M4. The gate-source voltage on M5 and M6 is low. As a result of the lower transformance and conditions, the latch's latency is longer.

There is only one tail current in this structure (only one current Mtail path). This determines the current and the differential amplifier for both the latch portion. You want a greater tail current to be able to regenerate quickly in the latch stage. On the other hand, one wishes a smaller tail current to keep transistors in poor inversion and to have a longer integration time (sampling time) and a better Gm/Id ration. Here sampling interval is the time interval in which differential amplifier provides gain (i.e. from (Vcom-Vth) to end of reset phase). Using a single tail current based comparator it is not possible and the optimization becomes very difficult. Internal node (between the differential amplifier and latch stage) is not at Vdd but at Vdd-Vth. Internal node voltages need to reset to supply voltage (Vdd)(which can be achieved by connecting extra reset transistor between Vdd and internal nodes) to increase integration time. In low voltage

operation, the total delay further increases. Moreover, the tail transistor Mtail operates mostly in the triode region. Hence, the tail current depends on input common-mode voltage, which is not desirable for regeneration. In the authors have presented the input flip voltage follower (FVF) is a current Comparator Architecture implementation rather than the input amplifier. The FVF provides advantages such as improved ICMR, high voltage swing capability, and class- AB service. The FVF has its own set of benefits. Since the FVF circuit has a voltage trailer, it has a low output impedance and can generate a relatively high voltage. Due to the FVF's dynamic biais current, its slew rate is high and its bigger tension swing provides the high resolution, resulting in a higher signal-over-noise ratio. The circuit is well-suited for medium-speed, high-speed, and low-voltage applications. Authors proposed a new low energy, high speed, low offset and small die size dynamic latch comparer architecture.

The key point in this comparator is to increase the volume to speed up conversion. Furthermore, the output stage is made up of a single pair of transistors with a lower load capacitance (CL) than other topologies. Based on the original two-stage tail-style comparator, a new, improved two-stage energy-efficient comparator is proposed. The input stage and latch stage of this architecture are separated to have low supply operation and are entirely dynamic without static power use. The authors present a new dynamic torque latch comparator with low power, high resolution, and low kickback noise. The suggested comparator has three phases. The first stage is an amplifier with two differential input pairs and diode loads. The second stage is the lock with the control switch and the final stage is easily locked using 2 back-to-back inverters and nMOS as a transistor intermediate. The transmission gate was used as a test (last latch) stage in the new power reduction technique. It is proposed to use a different input and a two-stage energy-efficient comparator based on the latch stage, which is based on the fundamental double-strength comparator. This architecture can be used with no static power consumption and a low supply voltage. The double tail lock is said to be supplemented by a symmetric low voltage high speed S-R latch.

CONCLUSION

We study and analysis a comprehensive delay and power analysis for clocked dynamic comparators is done and for that two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were studied and analyzed. Also, based on theoretical analyses, a new dynamic comparator with lowvoltage low-power capability was proposed in order to improve the performance of the comparator. Detailed analysis of performance parameters for the conventional dynamic latch comparators (referred comparators), viz. Single tail current dynamic latch comparator (STDLC), Double tail current dynamic latch comparator (DTDLC), Modified double tail current dynamic latch comparator (MDTDLC), two-stage dynamic comparator without an inverted clock (DTDLC-CLK), and Pre-amplifier with latch comparator (Pre+Latch) is carried out in this research . Various reset techniques are also discussed and analyzed for dynamic latch comparator and based on this study, a new reset technique (shared charge logic) is proposed to improve the speed and power of comparator. A new architecture of comparator with shared charge logic is proposed to improve the performance parameter of the dynamic latch comparator. Analytical expressions for the performance parameters are also derived. All these referred comparators and proposed comparator have been simulated in Cadence Virtuoso Analog Design Environment with 90 nm CMOS technology at 1 V of the supply voltage. Since, speed, power consumption, PDP, and die

area are trade-offs in terms of performance, primarily these parameters are simulated for the proposed.

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